Virtual Fabrication:
Integrated Process Modeling for Advanced Technology

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SEMICON West
San Francisco, CA
July 9, 2013
Process Cost and Complexity Increasing at Alarming Pace

Innovation is in structural integration – The challenge is PHYSICAL

New fab $5-10B, New process > $2B

This is all spent before a single revenue-generating wafer can be run

Much of process development cost is trial-and-error in-fab experimentation

A single cycle of experimental learning can cost $50M and take 3 months

Trial-and-Error Silicon Engineering is not acceptable!

The time and cost of TRIAL is too great

The penalty for ERROR is too extreme
What is SEMulator3D?

A Powerful 3D Semiconductor Virtual Fabrication Platform

- Applicable to ANY process & ANY layout
- Replaces build & test with **accurate** 3D modeling of large areas & complex process sequences
- Provides validation and visualization of relationships between design and process
- Provides a **predictive** view of design-technology interactions
Physics-driven etch modeling of
- Multi-material film stacks
- Multiple types of etch physics

Key Features
- Etch physics:
  - Redeposition (aka passivation)
  - Sputtering (physical etching)
  - Etch bias (lateral or chemical etching)

STI Etches

Spacer Etches

TFMHM-SAV M2 Overetch
Epitaxial growth is sensitive to crystal planes. 

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<111> directions normally grow slowest and form limiting facets.

22nm Tri-gate (Intel)

FinFET SiGe Epitaxy (<110> notched wafer)

FinFET SiGe Epitaxy (with residual oxide)

Embedded SiGe in planar technology (Intel, IBM)
Virtual Metrology Operations

- Automate in-line, local measurements of critical technology parameters
- Mimic real in-fab metrology
- Replace slow out-of-fab destructive characterization

**Expeditor** batch processing tool

- Automated, spreadsheet-driven massively parallel parameter studies

Example: DOE study on FinFET Epitaxy on <100> notched wafer: Dependence on pre-epitaxy fin erosion and epitaxial conditions
### Requirements:
- **Predictive** – Match actual fabrication process, and sensitivities
- **Ease of Use** – Deployed across large teams working on integration
- **Design-Aware** – Models must reflect intersection of design and process
- **Large Areas** – Integration challenges are larger than single transistors
- **Fast/Parallel** – Results faster than running wafer experiments

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**Obvious:** BEOL processes are pushed to the limit at 14nm

New patterning schemes to achieve density.
New metallization schemes for yield and reliability.

BUT...

1. High aspect ratio integration challenges
2. Variability becoming larger portion of nominal dimensions
3. Parasitic R/C trade-offs driving hierarchical BEOL
4. Next-node BEOL scaling remains non-trivial
Cross-Wafer Uniformity

- Unit process cross-wafer behavior is easily validated from inline metrology
- The cross-wafer requirement is integrated and electrical
  - Costly & time-consuming to verify on HW
- Typical practice involves individual process optimization, driving toward a “flat” profile for all processes
- SEMulator3D provides a predictive methodology for evaluating integrated structural results (using virtual metrology) due to multiple forms of variation across the wafer (using Expeditor)
  - Process Co-optimization
  - Intelligent APC

At 450mm, the cross-wafer effects will dominate, and new methodology will prevail
SEMulator3D models are the intersection of design and process. Integrated structural response to variations of multiple processes is now impossible to calculate with historical methods due to process complexity. Different designs respond to process variations differently. Virtual fabrication enables thorough investigation of design-process interaction.
Meshing allows use of realistic structures for electrical modeling.
**Obvious:** FinFET is the transistor architecture for the future of CMOS

Sub-threshold slope from double-gate structure improves power-performance

BUT...
1. 3D structural integration challenges
2. New variability sources: Body thickness/shape, epi, MOL, etc.
3. New parasitic R/C trade-offs
4. Next-node FET scaling remains non-trivial
MOL Variation Analysis

- Predictive process deck built using public TEMs
- Variation analysis using Expeditor batch tool

- Virtual Metrology extracting 3D interface surface area – would require out-of-fab destructive characterization
- Physical parameter serves as electrical sensitivity for resistance or reliability criteria
Meshing allows use of realistic structures for electrical modeling.
**Obvious:** Cost/bit NVRAM scaling has introduced **CRAZY** 3D structures

Vertical bit-line integration, multi-layer integration, etc.

**BUT...**
1. High aspect ratio integration challenges
2. Defects in multi-layer stack have wide-ranging implications
3. Further scaling drives more layers... really?!?!!?
**Macro-scale** – Example: Overall Integration  
Large multi-regional structure  
Complex multi-module integration

Modeling:  
- Large layout area selection  
- 1.0 nm resolution  
- Basic Etch Model

**Micro-scale** – Example: Plug Etch/Fill  
High aspect ratio etch  
Multi-layer cyclic etch process  
Profile details are critical

Modeling:  
- Layout area subset  
- 0.5 nm resolution  
- Advanced Etch Model

**SEMulator3D offers simple flexibility to explore different scales of physical challenges at high speed**
60nm metal defect embedded during early phases of multi-layer stack deposition

Defect “magnification” through remainder of stack deposition

Defect blocks “plug etch”, kills one bitline (expected). Plug module is robust enough for nearby bitlines to survive, despite non-planarity

Non-planarity affects “slit etch” later in flow. Results in underetch and shorted control gates. Kills entire sub-array block. NOT EXPECTED!!!

SEMulator3D enables defect evolution understanding for yield ramp calculation and optimization
A Virtual Learning Cycle

Utilize parallel computing infrastructure to dramatically accelerate development!

**Silicon Cycle of Learning:**
- Wafers: 40 WSD * 3 months
  - 150 5-way Experiments
  - All subject to variation
  - All captive to other processes
- Characterization: Additional Resource
- Analysis: Additional Resource
- Cost ~ $50M

**Virtual Cycle of Learning:**
- 150 Isolated 5-way Experiments
- 30 minute model build
  - High Resolution (~5A)
- 20 designs: Key Library Elements
- Characterization: Built-in (Virtual Metrology)
- Analysis: Pre-processed (Expeditor)
- 512 CPUs (4 CPUs/case): 2.4 days

**Parallel Model Build Time vs. CPUs**

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<td>POR</td>
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<td>S1 (3)</td>
<td>Process 1</td>
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<td>S2 (3)</td>
<td>Process 2</td>
</tr>
<tr>
<td>S3 (3)</td>
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<td>S4 (3)</td>
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Conclusion

• Advanced process technologies require Virtual Fabrication
  • Process complexity will impact Logic, SRAM, DRAM, Flash, etc.
• Process development in SEMulator3D saves time, money and development resources
• SEMulator3D Virtual Fabrication = more than visualization:
  • Cross-wafer process uniformity optimization and APC
  • Process centering conditions and sensitivity analyses
  • Meshing for electrical analysis such as Parasitic Extraction
  • Process corner analysis and design-process interaction sensitivities
  • Defect evolution exploration and yield-ramp optimization
• SEMulator3D capabilities benefit all semiconductor user groups:
  • Technology Developers: IDMs and Foundries
  • Fabless: Foundry Interface, IP Validation, DFM
  • Equipment/Process: Process co-optimization, APC, Integration context

Thank you for your time